Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-13 (canceled)

Claim 14 (original): A method for fabricating a semiconductor memory device comprising:

forming a pad on a semiconductor substrate;

forming an interlayer dielectric layer on the pad and semiconductor substrate for insulating the pad;

forming a bit line stack on the interlayer dielectric layer;

forming a pair of bit line spacers at both side walls of the bit line stack;

forming a storage node contact hole in the interlayer dielectric layer using a self align contact etching method, the storage node contact hole being aligned at the bit line spacers and exposing the pad; and

forming a multi-layered storage node contact plug in the storage node contact hole, by sequentially forming a first storage node contact plug and a second node contact plug in the storage node contact hole.

Claim 15 (original): The method for fabricating a semiconductor memory device of claim 14, wherein the first storage node contact plug is formed of a titanium nitride layer and the second storage node contact plug is formed of a polysilicon layer.

Claim 16 (original): The method for fabricating a semiconductor memory device of claim 14, further comprising forming a barrier metal layer on the second storage node contact plug, the barrier metal layer functioning as a third storage node contact plug.

Claim 17 (original): The method for fabricating a semiconductor memory device of claim 16, wherein the barrier metal layer is formed of one of a titanium nitride layer and a tantalum nitride layer.

Claim 18 (original): The method for fabricating a semiconductor memory device of claim 16, wherein the forming of the multi-layered storage node contact plug comprises:

forming a first storage node contact plug material layer on an entire surface of the semiconductor substrate after the storage node contact hole is formed, thereby partially filling the storage node contact hole;

forming a second storage node contact plug material layer on the first storage node contact plug material layer to sufficiently fill the storage node contact hole;

forming a second storage node contact plug in the storage node contact hole by etching back the second storage node contact plug material layer;

forming a barrier metal material layer on the entire surface of the semiconductor substrate on which the second storage node contact plug is formed; and

etching the first storage node contact plug material layer and the barrier metal material layer on the bit line stack.

Claim 19 (original): The method for fabricating a semiconductor memory device of claim 14, further comprising forming an ohmic layer on the pad and under the first storage node contact plug.

Claim 20 (original): The method for fabricating a semiconductor memory device of claim 19, wherein the ohmic layer is formed of one selected from the group consisting of titanium (Ti), cobalt (Co), molybdenum (Mo) and tungsten (W).